A GaAs SINGLE BALANCED MIXER MMIC WITH BUILT-IN ACTIVE BALUN FOR PERSONAL COMMUNICATION SYSTEMS

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ABSTRACT

A GaAs single balanced mixer IC with built-in active baluns for IF and LO inputs has been developed. The present mixer achieved the conversion gain of 16dB and the LO signal suppression over 30dBc at the LO input power of 0dBm. Owing to a novel BST (Barium Strontium Titanate) capacitor technology, the implemented mixer IC was packaged in the small 6pin outline with the extremely small chip size of 0.6 x 0.65mm^2. The IC can eliminate the LO filter of the up-conversion system for a variety of handyphone-sets in L-band.

INTRODUCTION

The GaAs microwave monolithic ICs (MMICs) have been widely used for personal communication systems in recent years because of their low voltage/ current operation capability. Mixer ICs used for those systems require to suppress various spurious signals such as a local oscillator (LO) signal particularly in transmitting block. So far, expensive and area-consuming filter is placed in the transmitting block to suppress the LO signal leakage. Otherwise, a balanced-type mixer configuration is adopted using a passive balun made of ferrite or microstripline [1]-[2]. However, such a filter or a balun requires large area that ends up with increasing the system size.

A variety of active balun circuits have been reported [3]-[5], however, these active baluns need large chip area because of the circuit complexity. In this work, we demonstrate a simple balun circuit which can extremely suppress the LO signal leakage by using a novel BST (Barium Strontium Titanate) capacitor technology [6]-[8].

The implemented single balanced mixer IC with built-in LO and IF baluns achieved the LO signal suppression over 30dBc with the conversion gain of 16dB at the supply voltage/current conditions of 3V/ 9.5mA.

CIRCUIT DESIGN

active balun

Figure 1 shows the configuration of the present active balun circuit where coupling capacitors of each 25pF are provided at the outputs using BST material. The output RFout1 and 2 should have equal amplitude and phase difference of 180°. Figure 2 shows the calculated relation between the phase unbalance for two outputs of the balun and the leakage of the undesired signal such as the LO signal. Taking into consideration of the system requirement that the LO leakage must be

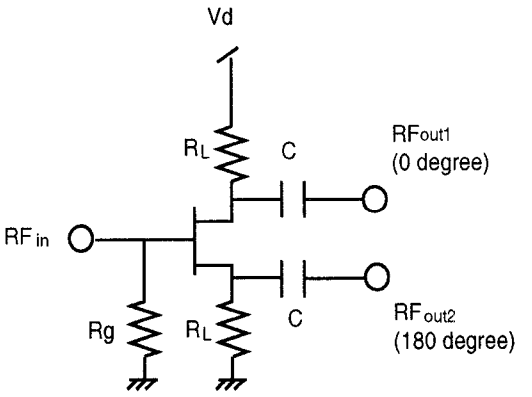

Figure. 1 Schematic circuit diagram of active balun.

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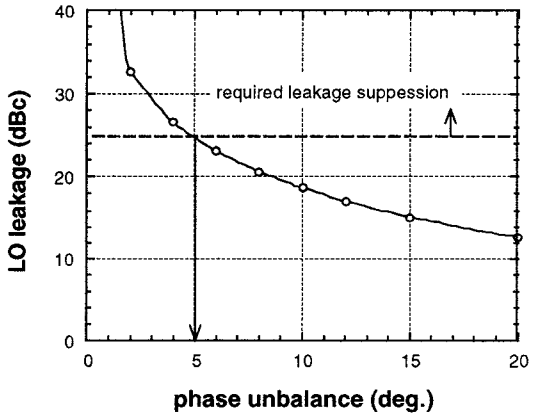

Figure 2. Simulated result of LO leakage for the phase unbalance.

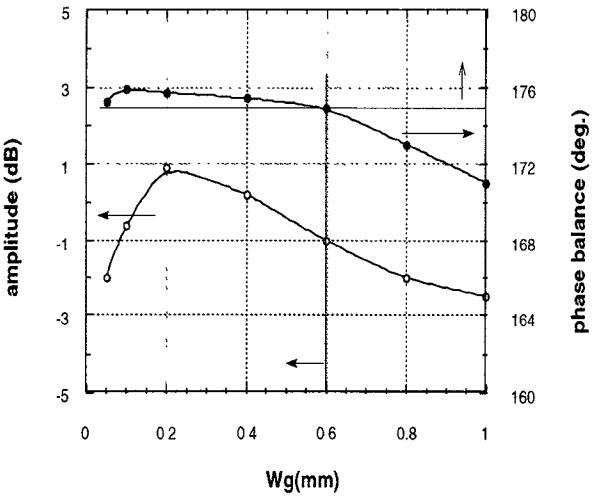

Figure 3. Amplitude and phase balance of the active balun output signal vs. gate width.
(FET device parameters : Lg=1μm, Vp=-0.6V, Idss=25mA, Cgs=0.2pF, Cgd=0.05pF with Vd=3V)

suppressed by more than 25 dBc that is equivalent to the typical LO filter. The phase unbalance must be within ±5° shown as a broken line in Fig.2.

Active devices such as an amplifier and a mixer are required to operate with a low supply voltage and a low current dissipation in personal communication systems. The supply voltage and the operating current are designed to be 3V and 3mA, respectively. We designed the residual drain-source voltage to be 2 V, where the good saturation characteristics is obtainable for the FET to obtain the optimum Cgs and Cgd. Therefore, the resistance value is designed to be 160Ω (≈ 0.5V/3mA).

The balance of the amplitude and phase for these two outputs are dependent on various parameters such as load resistances, gate-drain capacitance (Cgd) and a gate-source capacitance (Cgs) of the GaAs FET. In order to obtain the highest gain with small phase unbalance, we optimized the gate width of the FET. Figure 3 shows the simulated phase balance of the present active balun at the same current dissipation of 3mA varying gate width of the FET. You can see the phase balance is nearly constant within the gate width value of 50μm to 600μm, while the output signal amplitude of the active balun becomes the maximum value at 200μm. At this gate width, the phase unbalance on the present gate width is less than 4° that satisfies the above requirement of the LO leakage suppression of more than 25dBc. Therefore, the FET gate width is designed to be 200μm.

Mixer design

The single-ended balanced mixer is designed by combining two dual-gate FET with source-common self-biasing circuit. The mixer element is designed to obtain low distortion characteristics and high conversion gain. What should be designed for a single dual-gate FET mixer element is where the LO signal should be injected. Comparison of mixer performances as an up-converter for two cases of LO injection into the 1st gate and the 2nd gate is shown in Table I. You can see both the higher gain and better distortion characteristics are obtainable when the LO signal is injected into the 2nd gate.

TABLE I
Peformances of the dual-gate FET

LO injection port / performances	1st gate	2nd gate
Conversion Gain	9.8 dB	12.7 dB
Output IP3	4.0 dBm	4.8 dBm
LO leakage	-2.2 dBc	6.8 dBc

There is a optimum gate width and gate bias condition to obtain the minimum distortion condition at the limited current-consumption for the mixer element [9]. The optimized mixer FET has the gate width of 400μm at the current consumption of 3.5 mA.

The whole MMIC circuit is shown in Fig.4. Thus optimized baluns and dual-gate FET mixers are used to make a single balanced mixer. All the capacitors used in the present circuit are made of BST material which results in contributing the chip size reduction.

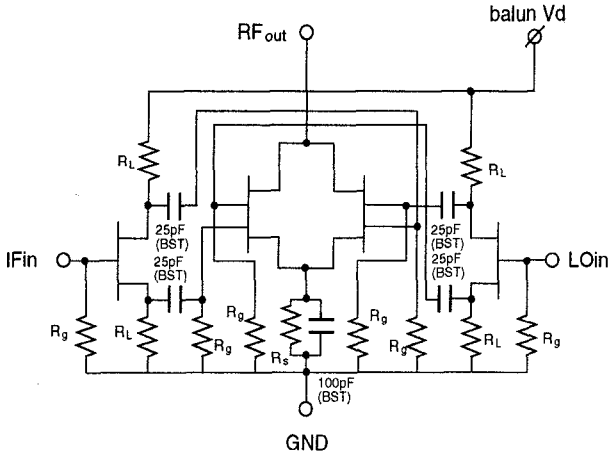

Figure 4. Mixer MMIC circuit diagram.

FABRICATION

The used FET has a gate length of 1μm. Used MESFETs are fabricated by using typical ion-implantation process. The BST capacitors have a dielectric constant of 300, which is about 50 times as large as the conventional SiN one [5]. The consumed area of those capacitors is reduced by the factor of 50.

A photograph of the fabricated single balanced mixer MMIC is shown in Fig.5. The resultant chip size is 650 x 600 μm^2. The MMIC is molded in a plastic 6pin-mini package that has foot-print of 2 x 3 mm^2.

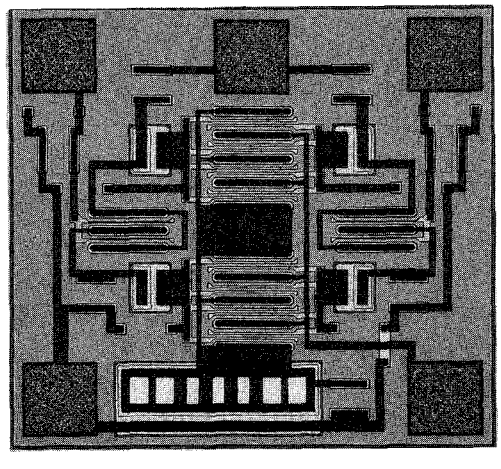

Figure 5. Photograph of mixer MMIC.

RF PERFORMANCE

Figure 6 shows the dependency of the up-mixing performance (conversion gain, LO leak, and NF) on the LO power at the IF and LO frequencies of 130 MHz and 950 MHz, respectively. It is noted that the input and output port are matched to 50 Ω using an external matching circuit. The conversion gain of 16dB, the noise figure of 5dB, and the LO leakage of more than 30dBc are achieved at the LO power of 0dBm. The resultant current dissipation of the present IC is 9.5mA at the supply voltage of 3V. The two tone intermodulation distortion characteristics of the fabricated mixer IC is shown in Fig.7. The obtained output third-order intercept-point of 7.5 dBm, which is at least 10 dB higher than Si one at the same voltage/current condition. Table II summarizes the performance of the present single-balanced mixer IC.

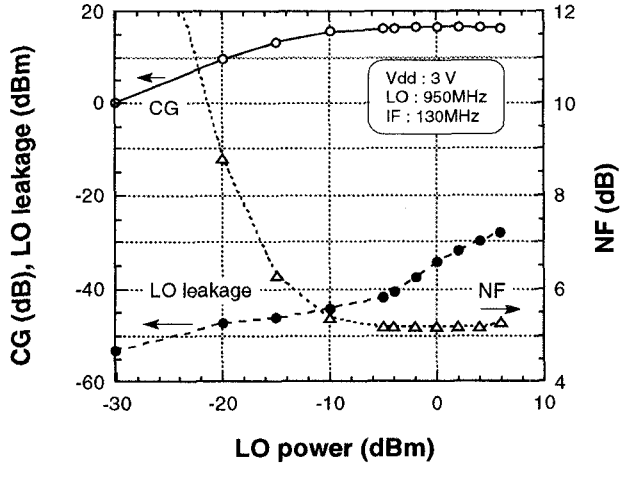

Figure 6. Coversion gain, LO leakage, and NF vs. LO power.

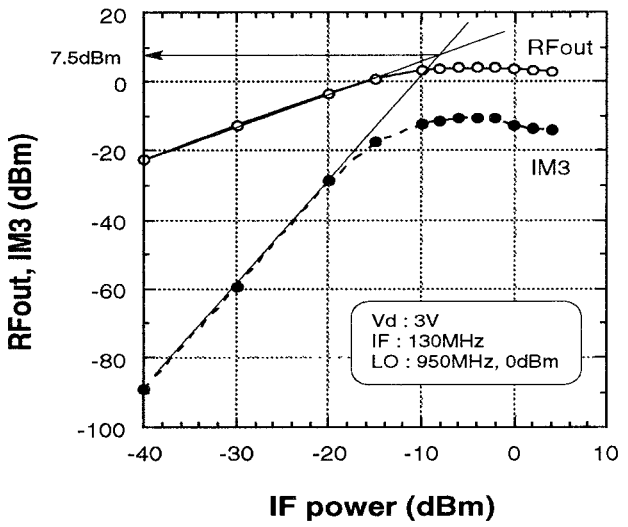

Figure 7. Input/output characteristics of mixer MMIC.

TABLE II
Performances of the single balanced mixer MMIC

Conversion Gain	16.7 dB
Noise Figure	5.2 dB
Output IP3	7.5 dBm
LO leakage	32.4 dBc
Supply voltage	3.0 V
Current dissipasion	9.5 mA

SUMMARY

The single balanced mixer with built-in active baluns which can suppress LO signal leakage of more than 30dBc have been successfully developed. This small LO leakage is good enough to eliminate the area-consuming LO filter. Owing to the novel BST capacitor technology, the implemented mixer IC was packaged in the small 6pin outline with the extremely small chip size of 0.6 x 0.65μm^2. The present MMIC is applicable to the various personal communication systems.

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